REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application. The independent claims have been amended to more clearly define the present invention over the cited prior art references. Support for the claim amendments may be found in paragraph 24 of the specification, for example. Certain dependent claims have been amended for consistency.

The claim amendments and arguments supporting patentablity of the claims are provided below.

I. The Amended Claims

The present invention, as recited in amended independent Claim 1, for example, is directed to a microprocessor comprising a processing unit, and a memory comprising a lower memory area and an extended memory area. An address bus connects the processing unit to the memory, and comprises a lower address bus for accessing the lower memory area and an extended address bus for accessing the extended memory area.

The microprocessor comprises means for executing instructions of an instruction set executable by the processing unit. The instruction set comprises instructions for accessing the addressable memory space. A first instruction group comprises instructions for accessing the lower memory area, and a second instruction group distinct from the first instruction group and only comprising all of the instructions for accessing the extended memory area. Means prevent the extended address bus from

accessing the extended memory area when executing an instruction in the first instruction group.

Independent device Claim 11 has been amended similar to amended independent device Claim 1, but without some of the means language. Independent method Claim 21 has been amended similar to amended independent device Claim 11.

II. The Claims Are Patentable

The Examiner rejected independent Claims 1, 11 and 21 over the Galvin et al. article. The Galvin et al. article is directed to operating system concepts. The Examiner cites Galvin et al. as disclosing a computer with two operating modes: a monitor mode and a user mode.

In the user mode, the processor has a limited access to a legal memory area. In the monitor mode, the processor has an unrestricted access to all the memory. In the user mode, any attempt to the memory outside the legal memory area is treated as a fatal error and triggers a trap routine.

In the claimed invention, the independent claims have been amended to recite that the microprocessor comprises an address bus comprising a lower address bus and an extended address bus for accessing respectively a lower and an extended memory area.

The Applicants submit that Galvin et al. fails to suggest a processor having an extended address bus for accessing an extended memory area. In contrast, the legal memory area cannot be restricted to a lower memory area since this area

contains the interrupt vectors that cannot be modified in the user mode. Further, the processor of Galvin et al. does not comprise a set of executable instructions divided into two groups, namely a group of conventional instructions accessing only to a lower memory area, and a second group comprising only all the instructions accessing to the extended memory area.

In sharp contrast, the privileged instructions of Galvin et al. are not disclosed as a group of instructions for accessing an extended memory area, and the instructions executable in the user mode are not restricted to access to the lower memory area which is a protected memory area since it contains interrupt vectors that cannot be modified in the user mode. In fact, an object of the Galvin et al. article is not to extend the memory space addressable by a processor, but to protect the operating system and other programs running in a computer when executing a user program.

Moreover, another object of Galvin et al. is not to maintain compatibility of old programs written for a processor that does not have an extended address bus, so that such old programs can be executed by a processor having an extended address bus. Also in sharp contrast with the claimed invention, the processor of Galvin et al. comprises two additional registers defining a memory area allocated to a user program, and means for controlling each memory access being requested by the user program is not outside the allocated memory area.

In the claimed invention, these means are not necessary since the instructions of the first group do not have an access

to the extended memory area: each location of the extended memory area is accessible using an address word which is longer than the address words for accessing a location of the lower memory area.

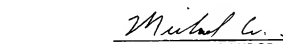
Accordingly, it is submitted that amended independent Claim 1 is patentable over the Galvin et al. article. Amended independent Claims 11 and 21 are similar to amended independent Claim 1. Therefore, it is submitted that these claims are also patentable over the Galvin et al. article.

In view of the patentability of amended independent Claims 1, 11 and 21, it is submitted that the dependent claims, which include yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

III. CONCLUSION

In view of the amendments to the claims and the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,



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